AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A power amplifier circuit comprising:

a first amplifier configured to receive an input signal, and in response, provide a first output signal;

a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input signal received by the first amplifier;

a second amplifier configured to receive the delayed input signal, and in response, provide a first delayed output signal;

an impedance inverter circuit configured to provide an impedance inversion and introduce a second delay to the first output signal, thereby creating a second delayed output signal;

a node connecting an output of the impedance inverter circuit and an output of the second amplifier, the node configured to combine the first and second delayed output signals, thereby creating an amplified output signal; ~~and~~

a level control circuit configured to provide a ~~first output~~ level control signal that causes the first amplifier to operate in a saturated mode when the first amplifier is enabled, and a second output level control signal that causes the second amplifier to operate in a saturated mode when the second amplifier is enabled; and

a bias control circuitry to enable the first and second amplifiers in response to the level control signal, wherein the bias control circuitry enables the first amplifier when the analog level control signal indicates a low power mode and enables both the first and second amplifiers when the analog level control signal identifies a high power mode.

2. (Currently Amended) The power amplifier of Claim 1, ~~further comprising~~ wherein the bias control circuitry ~~configured to~~ independently enables and disables the first and second amplifiers.

3. (Previously Presented) The power amplifier of Claim 2, wherein the bias control circuitry comprises a bias control circuit configured to generate a first bias voltage and a second bias voltage in response to an analog level control signal, wherein the first bias voltage is applied to the first amplifier and the second bias voltage is applied to the second amplifier.

4. (Currently Amended) The power amplifier of Claim ~~2~~ 3, wherein the bias control circuit comprises:

means for activating the first bias voltage and deactivating the second bias voltage when the analog level control signal identifies a low power mode; and

means for activating both the first and second bias voltages when the analog level control signal identifies a high power mode.

5. (Original) The power amplifier of Claim 1, wherein the first output level control signal and the second output level control signal are ramp signals.

6. (Canceled)

7. (Previously Presented) The power amplifier of Claim 1, wherein the first amplifier comprises a first transistor, and the level control circuit comprises a first control transistor coupled between a collector of the first transistor and a voltage supply terminal.

8. (Original) The power amplifier of Claim 7, further comprising an inductor coupled between the collector of the first transistor and the first control transistor.

9. (Previously Presented) The power amplifier of Claim 7, wherein the second amplifier comprises a second transistor, and the level control circuit comprises a second control transistor coupled between a collector of the second transistor and the voltage supply terminal.

10. (Original) The power amplifier of Claim 9, further comprising:

an inductor coupled between the collector of the first transistor and the first control transistor; and

an inductor coupled between the collector of the second transistor and the second control transistor.

11. (Original) The power amplifier of Claim 1, wherein the first delay circuit comprises an inductor and one or more capacitors.

12. (Original) The power amplifier of Claim 11, wherein the impedance inverter circuit comprises an inductor and one or more capacitors.

13. (Previously Presented) The power amplifier of Claim 1, wherein the first amplifier comprises at least one heterojunction bipolar transistor, and wherein the second amplifier comprises at least one heterojunction bipolar transistor.

14. (Original) The power amplifier of Claim 1, wherein the first delay is equal to the second delay.

15. (Currently Amended) A method of amplifying an input signal, comprising:

providing the input signal to a first amplifier;

applying a first bias voltage to a base of the first amplifier to enable the first amplifier in response to a level control signal;

applying a first output level control signal to a collector of the first amplifier to cause the first amplifier to operate in saturated mode when the first amplifier is enabled, such that the first amplifier provides a first output signal in response to the input signal;

introducing a first delay to the input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input signal received by the first amplifier;

providing the delayed input signal to a second amplifier;

~~enabling~~ applying a second bias voltage to a base of the first amplifier to enable the first amplifier in response to another level control signal to enable the second amplifier to operate in a saturated mode, wherein the second amplifier provides a first delayed output signal in response to the delayed input signal;

introducing a second delay to the first output signal, thereby creating a second delayed output signal; and

combining the first and second delayed output signals at an output node of the second amplifier, thereby creating an amplified output signal.

16. (Original) The method of Claim 15, further comprising selecting the first delay to be equal to the second delay, such that the first and second delayed output signals are substantially in phase.

17. (Previously Presented) The method of Claim 15, further comprising disabling the second amplifier in a low power mode.

18. (Canceled)

19. (Previously Presented) The method of Claim 15, wherein the first output level control signal is a ramp signal.

20. (Previously Presented) The method of Claim 17, wherein the step of enabling the second amplifier to operate in a saturated mode comprises:

applying a second bias voltage to a base of the second amplifier; and

applying a second output level control signal to a collector of the second amplifier.

21. (Original) The method of Claim 20, wherein the second output level control signal is a ramp signal.